Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A single track-and-hold circuit having an input signal (Vin) and an output signal (Vs), a bootstrap switch (14a) having as its inputs a clock signal (clk) and an input signal (vin), said input signal (vin) of said bootstrap switch (14a) being connected to said output signal (Vs) of said circuit via a current source (20) and a buffering transistor (30), characterized in that said input signal (vin) of said bootstrap switch (14a) comprises said output signal (Vs) of said circuit; said single track-and-hold circuit further comprising a capacitor (12), said input signal (Vin) being connected to said capacitor (12) via a switch (10), said switch (10) being closed during a track mode of said circuit and open during a hold mode of said circuit, said bootstrap switch (14a) having as an output to said switch (10), a clock signal (clkboot) equal to said input signal (Vin) added to a supply voltage (Vdd); ~~and~~

including a second bootstrap switch (14b), the input signal (vin) of which is connected to said output signal (Vs) of said single track-and-hold circuit via said current source (20) and said buffering transistor (30) of said single track-and-hold circuit; and

two dummy switches (16) connected on either side of said switch (10) and clocked in anti-phase to said switch (10) by anti-phase boot clock signal (clknboot);

wherein both said bootstrap switch (14a) and said bootstrap switch (14b) are connected to the same level shifted output signal (Vs).

2. (canceled)

3. (previously presented) A single track-and-hold circuit according to claim 1, wherein said buffering transistor (30) comprises a MOS transistor.

4. (previously presented) A single track-and-hold circuit according to claim 3, wherein said MOS transistor (30) is a PMOS transistor.

5. (canceled)

6. (canceled)

7. (canceled)

8. (original) An analog-to-digital converter including a track-and-hold circuit according to claim 1.

9. (original) An integrated circuit including an analog-to-digital converter according to claim 8.

10. (new) A single track-and-hold circuit according to claim 1, wherein Vgs of switch (10) is equal to Vdd + Vlevelshift.

11. (new) A single track-and-hold circuit according to claim 1, wherein Vgs of switch (10) is equal to Vdd + 0.5V.

12. (new) A single track-and-hold circuit according to claim 1, wherein said output signal (Vs) is constant in hold mode so there is no crosstalk to said capacitor (12).